REMARKS

This amendment responds to the first office action. Claims 71-75 and 77-85 have been amended, and new claims 86-100 have been added.

The Examiner has requested that applicants update the status of the parent application. Applicants note that the parent application Serial No. 07/389,334 has issued as U.S. Pat. No. 5,440,749. Also pursuant to the Examiner's request, a new title and new abstract more aptly descriptive of the invention have been provided.

The Examiner has rejected claims 71-85 under 35 U.S.C. § 112 as being indefinite. With respect to claim 71, the Examiner asserted that although instructions were fetched for the CPU, means were not recited for supplying the fetched instructions to the CPU. It was also stated that the functional interaction between the counter and the instruction supplying means was unclear. In addition, at pages 2 and 3 of the Office Action, the Examiner deemed various instructions recited in claims 72-79 and 82-83 to be unclear.

Applicant has carefully considered the issues raised by the Examiner and has endeavored to amend the claims so as to achieve compliance with 35 U.S.C. § 112. For example, claim 71 now recites that the instruction supplying means is disposed to supply, in succession from said instruction register, the one or more sequential instructions of a first of the instruction groups to the central processing unit. Hence, the pending claims now provide a mechanism for supplying the instructions from the instruction register to the central processing unit. See, for example, FIG. 20 in which *instruction supplying means* including decoder 440 and gates 442 selectively couple instructions from register 108 for use by the microprocessor.

Although claim 71 has been amended to omit reference to the previously claimed "counter", this element remains recited in claims 74 and 82. The counter 180 is described in the specification at page 33, and is shown in FIG. 16 to be responsive to increment/decrement/reset signals provided by the instruction decoding means. Signals produced by the counter 180 are used by decoder 440 to control gating (442) of instructions from the instruction register 108 to the central processing unit via the address bus (FIG. 20).

Hence, the function of the claimed counter is well-defined within the specification and drawings.

In response to the Examiner's commentary regarding the lack of clarity and antecedent basis inherent within claims 72-79 and 81-83, alternate language has been incorporated therein so as to more distinctly claim the invention which appears to be available for protection. Accordingly, applicant respectfully submits that the pending claims comport with the requirements of 35 U.S.C. § 112, and requests that the outstanding rejection thereunder be withdrawn.

The Examiner has rejected claims 71-73, 78-80 and 82-85 under 35 U.S.C. § 103 as being unpatentable over Boufarah. With respect to claim 71, the Examiner states that Boufarah teaches a microprocessor system comprising:

a CPU 20,
a memory 10,
a bus,
instruction fetching means 14,
an instruction register 934, 36 and 38,
instruction supplying means 14,
a counter (inherent program counter), and
instruction decoding means (processors 20 and 22)

Applicant observes that Boufarah describes a system in which instruction register (36,38) stores a sequence of instructions, and in which buffer control logic 40 determines whether the instruction sequence includes a branch instruction (Abstract, FIG. 3). If a branch instruction is detected in the instruction register, various other actions may then be taken (Abstract).

In Boufarah's system, only instructions appear to be stored within the instruction register (36, 38). See, for example, FIGS. 2a-2j, which shows the various instructions X1-X3, T1-T8, BRU, etc., loaded into instruction register 36. This contrasts with the system of invention, in which instructions as well as operands of variable-length are loaded into instruction register 108. See, e.g., the specification at pages 42-43, which describes the inclusion of 8, 16 and 24-bit operands (YYYYYYYY) within the instruction register 108 along with instruction op-codes (WWWWWWWW). These instructions/operands within the

instruction register are then provided to the central processing unit via an address or data bus as follows:

> ... The microinstruction counter 180 selects which 8-bit instruction to execute. If a JUMP or IMMEDIATE instruction is decoded, the *state of the 2-bit microinstruction counter selects the required 8, 16, or 24 bit operand* onto the address or data bus. The unselected 8-bit bytes are loaded with zeros by operation of decoder 440 and gates 442. The advantage of this technique is the saving of a number of op-codes required to specify the different operand sizes in other microprocessors. (page 33, lines 19-28)

The system of the invention further differs from Boufarah's system in that, for instructions requiring operands, the instruction's position within the instruction register is indicative of the width of the associated operand. This feature of the invention is described at page 43, lines 13-15:

> ... The microprocessor instruction decoder *figures out the width of the operand field by the location of the instruction op-code* in the four bytes [of the 32-bit instruction register 108]

By this amendment the claims have been amended to highlight the foregoing features and advantages of the present invention. For example, claim 71 now recites instruction decoding means for configuring the instruction supplying means to select from the instruction register an operand associated with a particular instruction of a given instruction group. This aspect of the present invention is described in the foregoing excerpt from the specification at page 33, and may be further appreciated with reference to FIGS. 16 and 20. Specifically, instruction decode logic and counter 180 cooperate to generate an operand selection signal provided to decoder 440. In turn, decoder 440 causes gates 442 to select the appropriate operand from register 108 for placement on the bus. Again, Boufarah does not suggest the selection of operands from the register nominally used to store instructions.

Claim 73 has been amended to more particularly identify the aspect of the present invention described in the specification at pages 46 and 47. Namely, claim 73 is directed to conditional SKIP instructions (e.g., SKIP-IF-ZERO, SKIP-IF-NO-CARRY), in which the response to the SKIP instruction depends upon the existence of a predefined condition.

Accordingly, applicant respectfully submits that pending claims 71-73, 78-80 and 82-85 are patentably distinguishable from Boufarah, and thus respectfully requests withdrawal of the rejection of these claims under 35 U.S.C. § 103.

At page 5 of the Office Action, claims 74-77 and 81 were rejected under 35 U.S.C. § 103 as being unpatentable over Boufarah in view of May. Although the Examiner asserts that May teaches loop and SKIP instructions, applicant respectfully submits that Boufarah in combination with May fails to suggest the loop or SKIP operations contemplated by the pending claims. In particular, claims 74-77 and 81 depend directly or indirectly from claim 71, and neither Boufarah nor May describe the system of claim 71; that is, a system in which operands are selected from an instruction register disposed to contain both operands and instructions. Moreover, neither Boufarah nor May appear to suggest the specific features of claims 74-77 and 81. For example, these references fail to suggest the system of claim 74, which recites that a decrement signal is provided to the loop counter in response to a MICROLOOP instruction within instruction register. See, e.g., FIG. 16 and the description of the decrement signal at page 49, lines 28, 34, and page 50, lines 7, 15, and 23.

Accordingly, applicant respectfully submits that pending claims 74-77 and 81 are patentably distinguishable from Boufarah in view of May, and thus respectfully requests withdrawal of the rejection of these claims under 35 U.S.C. § 103.

New claims 86-100 have been added in order to alternately identify the invention which appears to be available for protection. For example, new claim 87 is directed to the SKIP ALWAYS instruction in which instructions remaining within the instruction register are skipped, and a new instruction group is fetched from memory. In new claim 88, it is specifically recited that the width of an operand within the instruction register is related to the position of a particular one of the instructions within the instruction register.

Accordingly, in view of the above remarks, it is submitted that this application is now ready for allowance. Early notice to this effect is solicited.

If in the opinion of the Examiner, a telephone conference would expedite the

prosecution of the subject application, the Examiner is invited to call the undersigned at (415) 843-5000.

Respectfully submitted,

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